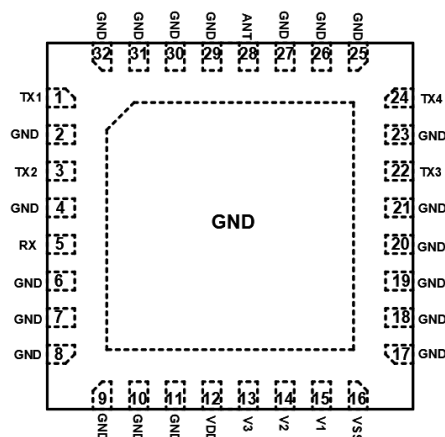


性能特点

- 工作频率: DC - 3 GHz
- 工作模式: SP5T或SP3T
- RX插入损耗: 0.80 dB @ 1.5 GHz
- TX插入损耗: 0.80 dB @ 1.5 GHz
- TX-RX隔离度: 42 dB @ 1.5 GHz
- TX-TX隔离度: 42 dB @ 1.5 GHz
- IP0.1 dB: 43 dBm
- 32-pin 4 mm × 4 mm × 1 mm QFN leadless package

引脚定义



俯视透视图

产品简介

ADIC421LP4是一款SOI CMOS MMIC单刀五掷开关, 频率范围覆盖DC - 3 GHz, 插入损耗0.80 dB, 隔离度42 dB, 输入功率0.1 dB压缩点43 dBm。采用32-pin 4 mm × 4 mm × 1 mm QFN leadless 封装, 可广泛应用于RF/微波电路和测试测量。

推荐工作条件

VDD	+3.4 V to +5.5 V
VSS	-3.6 V to -3.2 V
控制电压	High = 3.3 V Low = 0 V

极限参数

输入功率	45 dBm
电源电压 VDD	+3.4 V to +5.5 V
工作温度	-40 °C ~ 125 °C
存贮温度	-65 °C ~ 150 °C
防潮等级	1

引脚编号	符号	功能描述
1	TX1	发射引脚1
3	TX2	发射引脚2
5	RX	接收引脚
12	VDD	供电电压
13	V3	控制电压3
14	V2	控制电压2
15	V1	控制电压1
16	VSS	外部负电压控制
22	TX3	发射引脚3
24	TX4	发射引脚4
28	ANT	Antenna公共端
其他	GND	接地

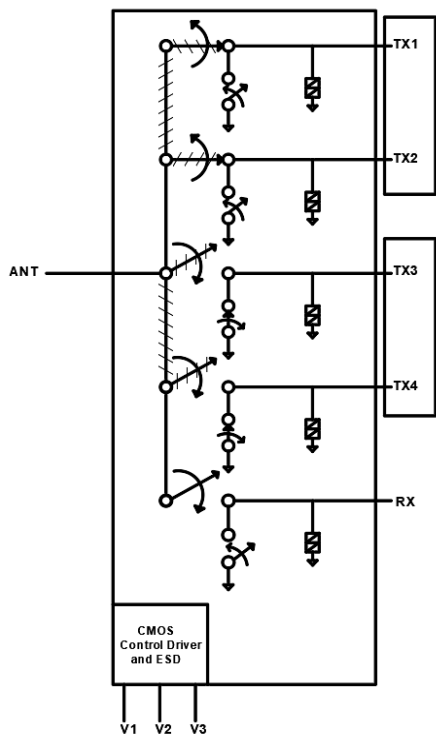


关注公众号

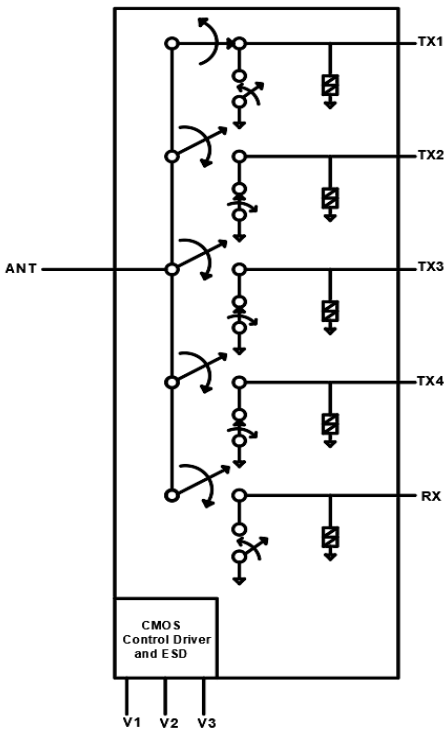
ADIC421LP4

V0

功能原理图

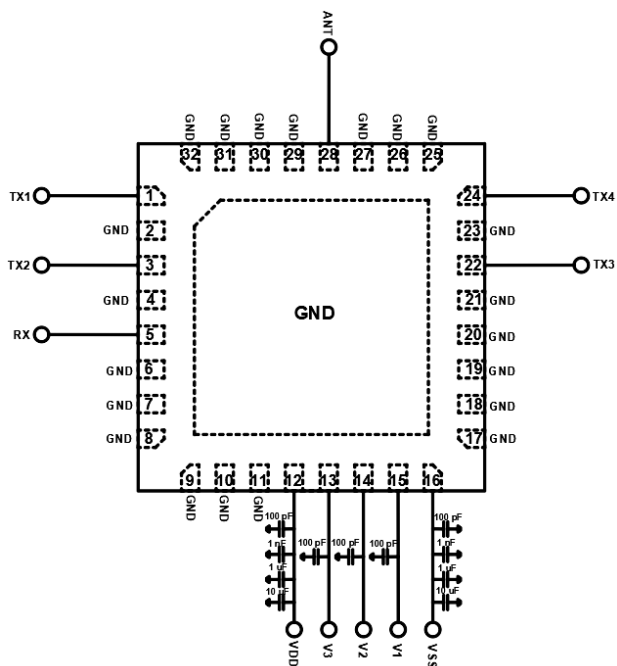


SP3T模式：TX1和TX2、TX3和TX4合并使用



SP5T模式

应用电路



说明：

- 1) VDD工作范围+3.4 V ~ +5.5 V;
- 2) VDD与VSS加100 pF, 1 nF, 1 uF, 10 uF 四个滤波电容;
- 3) V1、V2、V3加一个100 pF滤波电容;
- 4) 射频端口不需要加隔直电容。

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V0

电性能表 (T = 25 °C, VDD = +3.4 V ~ +5.5 V, VSS = -3.4 V, VH = +3.3 V, VL = 0V, 50 Ω系统)

指标	最小	典型	最大	单位	范围
插损 (ANT-TX)	-	0.5	0.9	dB	DC - 1.5 GHz
	-	1.2	1.5	dB	1.5 - 3.0 GHz
插损 (ANT-RX)	-	0.6	0.8	dB	DC - 1.5 GHz
	-	0.8	1	dB	1.5 - 3.0 GHz
隔离度 (TX-TX)	43	53	-	dB	DC - 1.5 GHz
	35	38	-	dB	1.5 - 3.0 GHz
隔离度 (TX-RX)	43	48	-	dB	DC - 1.5 GHz
	35	38	-	dB	1.5 - 3.0 GHz
回波损耗 (ANT)	10	12	-	dB	DC - 1.5 GHz
	7	8	-	dB	1.5 - 3.0 GHz
回波损耗 (TX)	9	13	-	dB	DC - 1.5 GHz
	7	9	-	dB	1.5 - 3.0 GHz
回波损耗 (RX)	12	15	-	dB	DC - 1.5 GHz
	12	14	-	dB	1.5 - 3.0 GHz
输入0.1 dB压缩点 (CW)	-	43	-	dBm	

真值表

状态	V3	V2	V1
ANT-TX1	L	L	H
ANT-TX2	L	H	L
ANT-TX1 and TX2	L	H	H
ANT-RX	H	L	L
ANT-TX3	H	L	H
ANT-TX4	H	H	L
ANT-TX3 and TX4	H	H	H

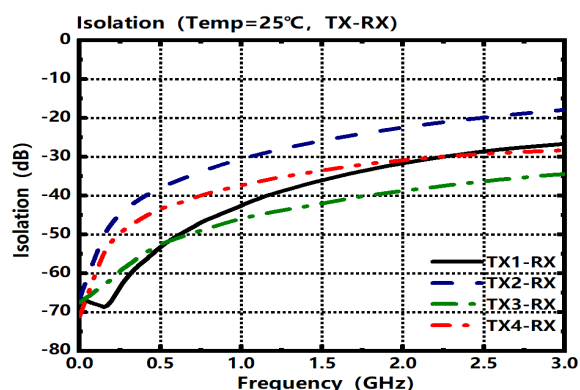
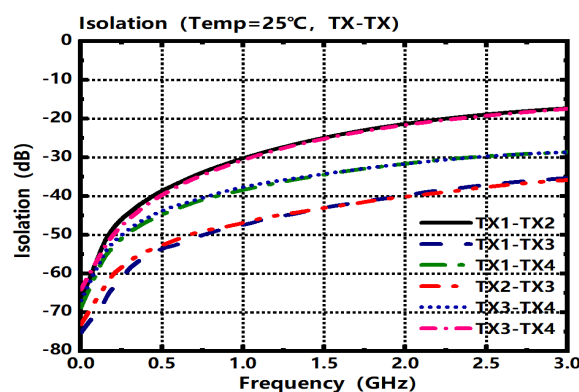
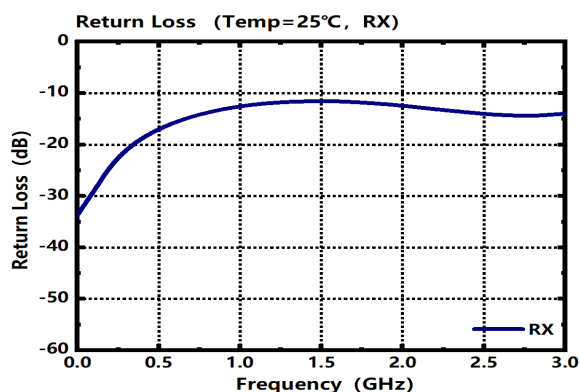
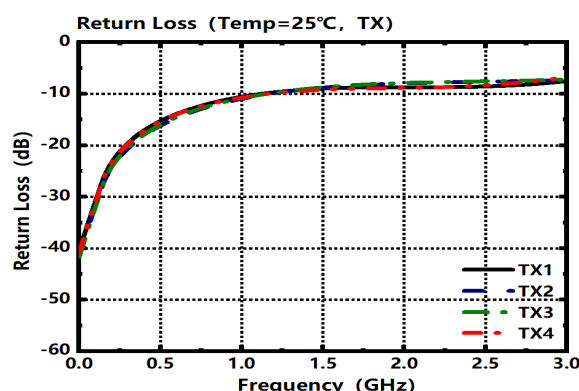
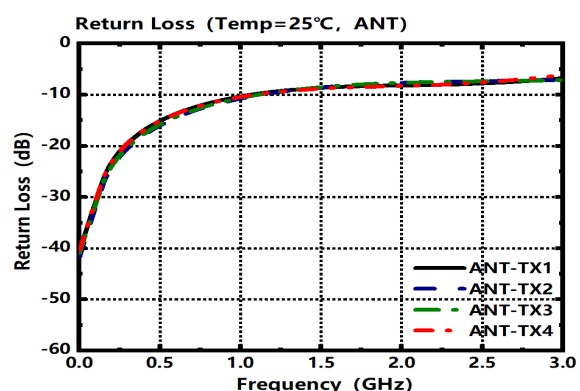
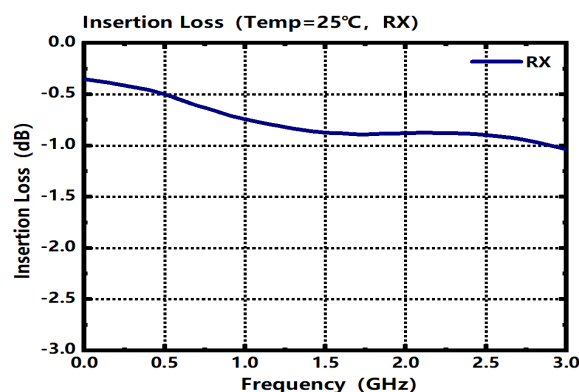
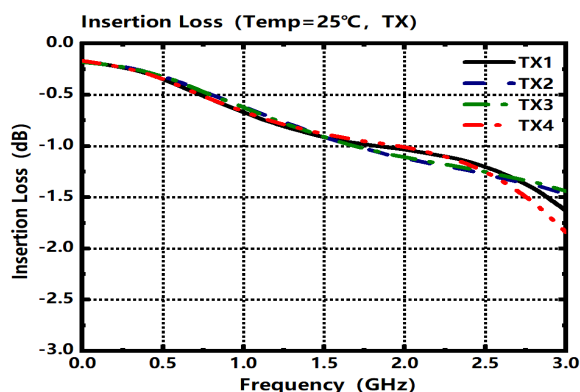
High = 3.3 V

Low = 0 V

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V0

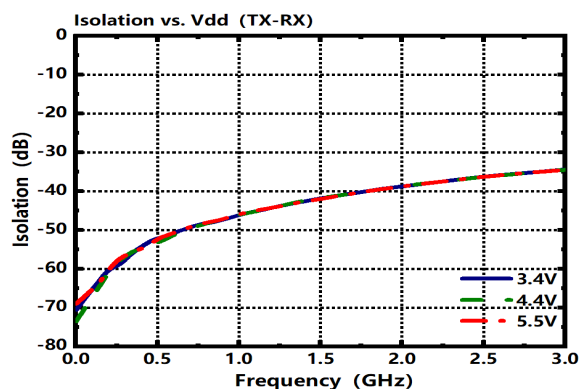
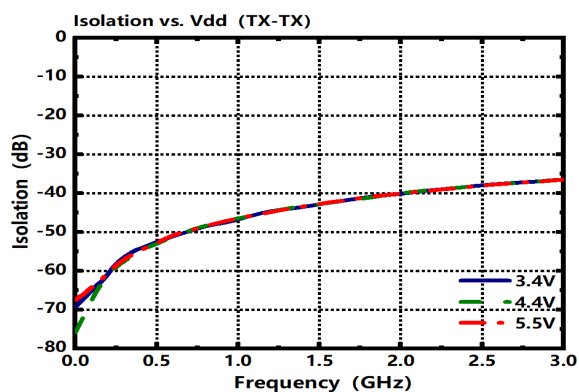
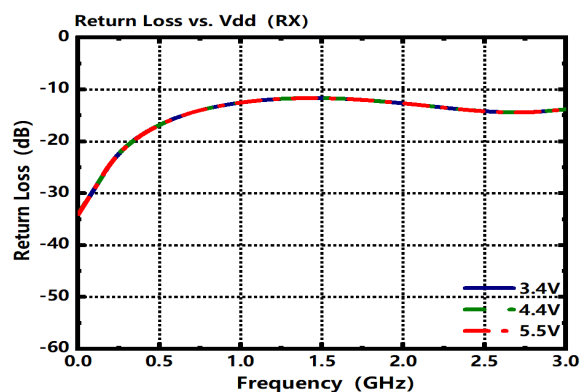
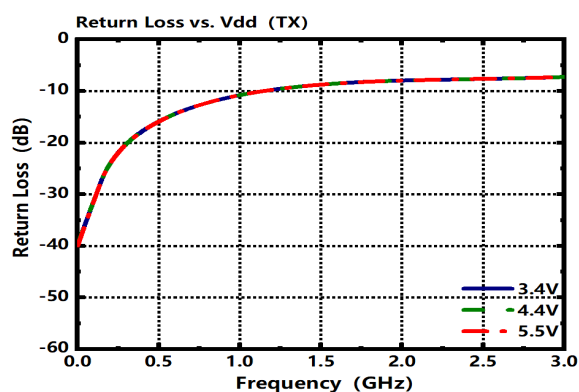
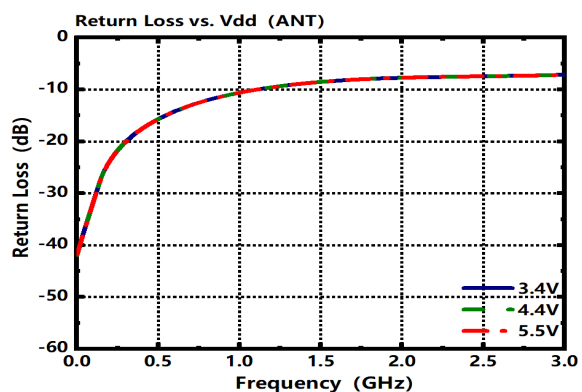
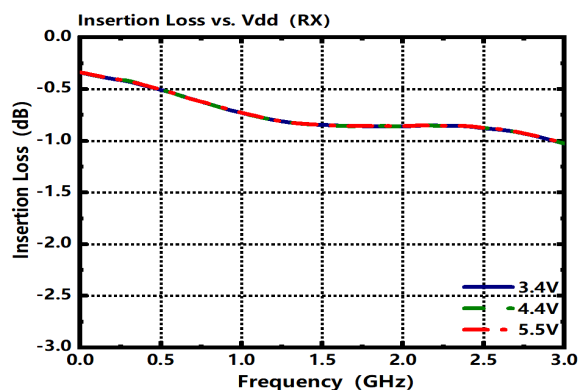
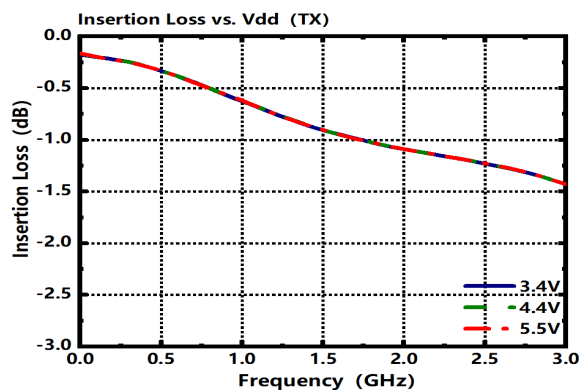
典型测试曲线 (T = 25 °C, VDD = +3.4 V, VSS = -3.4 V, VH = +3.3 V, VL = 0V, 50 Ω系统)



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V0

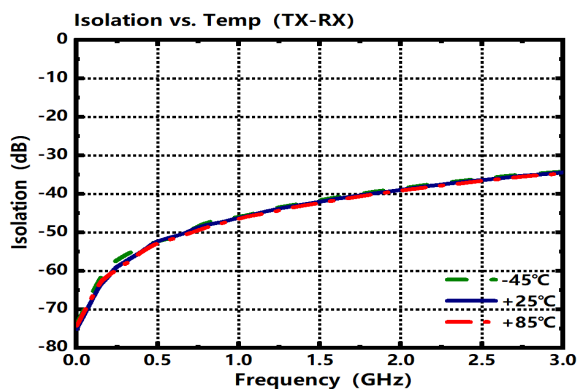
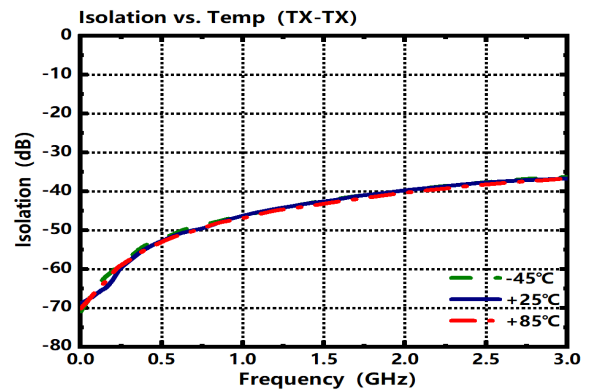
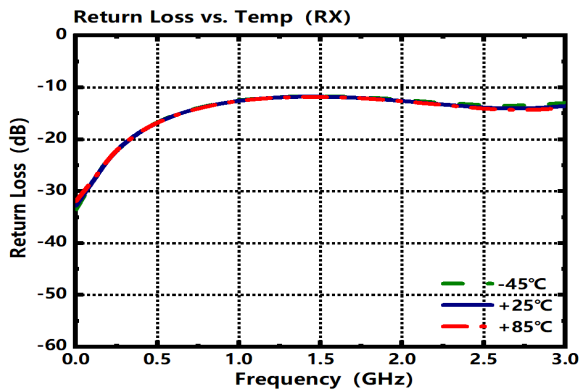
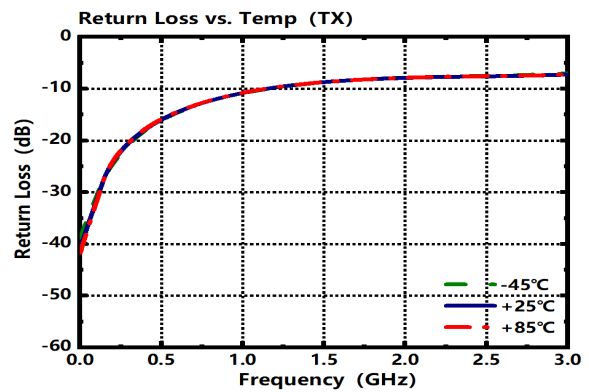
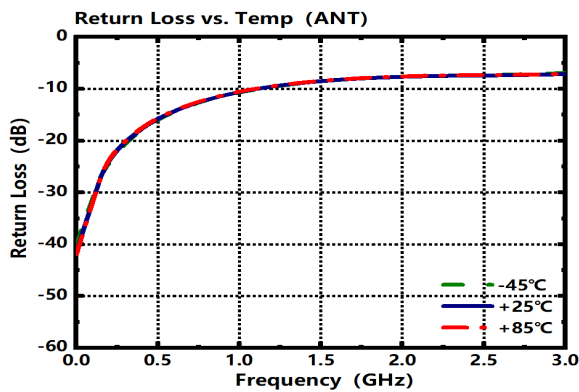
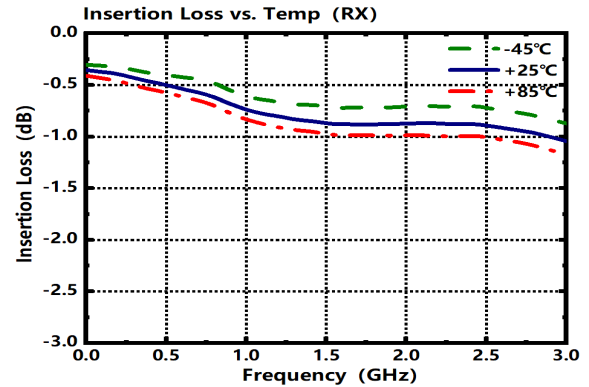
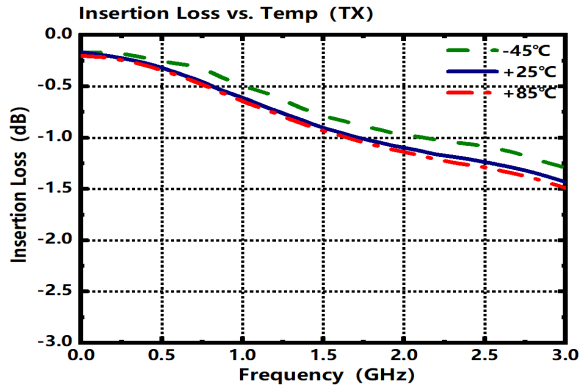
典型测试曲线 ($T = 25\text{ }^{\circ}\text{C}$, $V_{DD} = +3.4\text{ V} \sim +5.5\text{ V}$, $V_{SS} = -3.4\text{ V}$, $V_H = +3.3\text{ V}$, $V_L = 0\text{ V}$, $50\text{ }\Omega$ 系统)



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V0

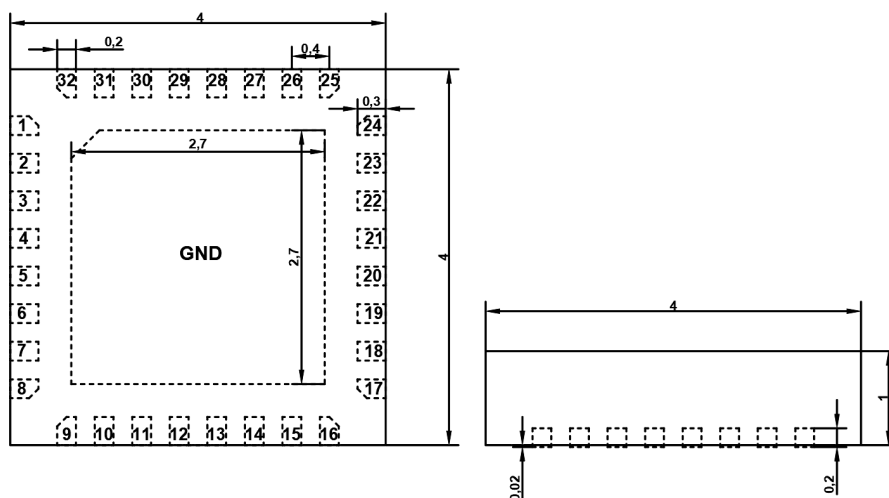
典型测试曲线 (高低温测试, $V_{DD} = +3.4\text{ V}$, $V_{SS} = -3.4\text{ V}$, $V_H = +3.3\text{ V}$, $V_L = 0\text{ V}$, $50\ \Omega$ 系统)



ADIC421LP4

V0

外形尺寸



俯视透视图

单位: mm

侧视图

建议引脚PCB

